1. Verilog

   a. Implement using AND and OR gates (and possible inverters) the circuit described by the Verilog code below

   ```verilog
   module muxi(S, D0, D1, y);
   input S, D0, D1;
   output y;
   assign y = S ? D1 : D0;
   endmodule
   ```

   b. Convert the circuit to NAND/NOR + inverters (use DeMorgan’s Law)

2. Design exercise

   Design a device that has one, two or more digital inputs (normally closed - NC), and it is triggered by opening of one of the contacts. It should be possible to expand the number of contacts as well as have the switch to configure the contacts to normally open – NO.

   The device should count two (or more i.e. adjustable number) of triggerings within a time interval (e.g. 30 sec., but the time should also be adjustable). In case an event is registered, an NC contact is activated.

   The voltage supply is 5V. You can use 555 circuit to generate clock, you can use any sequentials and combinational circuit – flip-flops, gates, counters, multiplexers, encoders, decoders etc., but a simple solution is highly appreciated.